

Software Specifications

Get to know more about the D1000 Series Portable Desktop with a detailed look at the software specifications.

The information contained in the chapter can be quite useful when you are troubleshooting the system's hardware. Each item has its individual usage for you to understand the software side of the Portable Desktop's architecture. This chapter includes specifications about:

- System features
- BIOS Specifications

1. General Description

The specification is a guideline for bios development on D1 platform. It is for internal use only. Anyone who need the system bios information can check this document for reference.

The general device specification, hardware block diagram, SMBUS, PCI Devices IRQ Routing Table, GPIO definition and so on are subjected to be depicted in this document. Hotkeys implementation and other bios features are also included in the document.

SOFTWARE SPECIFICATIONS

1. 2. CPU, Chipsets & Main Devices

Table 2-1

Item	Vendor	Specification	Part's Name	Revision
CPU	Intel		Northwood	B0/C1
North Bridge	SiS		650M	
South Bridge	SiS		962	
VGA	SiS		650M	
Audio Codec	Realtek		ALC650	
Modem Codec	Lucent			
USB	SiS		962	
Lan	Broadcom		BCM4401KFB	
Cardbus	ENE		CB710	
IEEE1394	SiS		962	
AC97 Controller	SiS		7012	
MC97 Controller	SiS		7013	
Glock Gen.	ICS		952003AF	
SIO	ITE		IT8705F	

3. PCI Devices & Interrupt Routing Table

Table 3-1

Device	Vendor	Bus #	Device #	Function #	INTA	INTB	INTC	INTD	INTE	INTF	INTG	INTH
Host bridge	SiS	0	0	0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PCI2PCI Bridge	SiS	0	1	0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
USB	SiS	0	3	0	N/A	N/A	N/A	N/A	*PIRQA	N/A	N/A	N/A
USB	SiS	0	3	1	N/A	N/A	N/A	N/A	N/A	*PIRQB	N/A	N/A
USB	SiS	0	3	2	N/A	N/A	N/A	N/A	N/A	N/A	*PIRQC	N/A
USB	SiS	0	3	3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	*PIRQD
LPC Bridge	SiS	0	2	0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
IDE	SiS	0	2	5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SMBus ¹	SiS	0	2	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Audio	SiS	0	2	7	N/A	N/A	*PIRQC	N/A	N/A	N/A	N/A	N/A
Modem	SiS	0	2	6	N/A	N/A	*PIRQC	N/A	N/A	N/A	N/A	N/A
IEEE 1394	SiS	0	2	3	N/A	*PIRQB	N/A	N/A	N/A	N/A	N/A	N/A
VGA	SiS	1	0	0	PIRQA	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Lan	Broadcom	0	15	0	PIRQC	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Cardbus slot	ENE	0	16	0	PIRQA	PIRQD	N/A	N/A	N/A	N/A	N/A	N/A

* : DEVICE INTERNAL ROUTING

¹ : Device Hidden

4. GPIO Definition Tables

The following tables are the definition of GPIO pins which included of south bridge(SIS962), KBC(KB3886) and super IO(IT8705F). Some of GPIO pins need to be initialized by system BIOS and some of them need the driver to support. Please check the Description column for reference.

Table 4-1. SIS962 GPIO Definition

GPIO	Type	Multi-function	Definition	Activated Level	Description
0	O	GPIO0/SPDIF	BIT0	N/A	CPU Vcore over-voltage BIT0
1	O	GPIO1/LDRQ1#	BIT1	N/A	CPU Vcore over-voltage BIT1
2	I	GPIO2/THERM#	THERM#	Low	NOTIFY SYSTEM THE THERMAL EVENT
3	I	GPIO3/EXTSMI#	EXTSMI#	Low	From KBC, notify system the SMI event
4	O	GPIO4/CLKRUN#	GPO4	N/A	N/A
5	O	GPIO5/PREQ5#	POW	High	Disable auto power off function
6	O	GPIO6/PGNT5#	GP6	High	Enable KBC SCI
7	I	GPIO7	GPWAKE	Low	Audio DJ power button
8	I	GPIO8/RING	LID#	Low	LID switch off
9	O	GPIO9/AC_SDIN2	KBC SCI	High	From KBC, notify system the SCI

SOFTWARE SPECIFICATIONS

					event
10	N/A	GPIO10/AC_SDIN3	N/A	N/A	N/A
11	O	GPIO11	BACK_OFF#	Low	Turn off the LCD back light
12	I	GPIO12/CPUSTP#	CPUCD#	Low	A preliminary control signal intends to put CPU into low frequency mode
13	I	GPIO13/DPRSLPVR	VCORECD#	Low	A PRELIMINARY CONTROL SIGNAL INTENDS TO PUT CPU INTO LOW FREQUENCY MODE
14	I	GPIO14	BATIN#	Low	High/Low: AC adapter/Battery
15	O	GPIO15	N/A	N/A	N/A
16	O	GPIO16	N/A	N/A	N/A
17	O	GPIO17	N/A	N/A	N/A
18	O	GPIO18	N/A	N/A	N/A

* : PU -> Pull Up, PD -> Pull Down, NC -> Not Connected

¹: powered in resume well.

5. Devices

5.0 – CPU

Intel P4 is designed in the D1 system.

5.1 - NORTH BRIDGE (SIS650M)

5.1.1 – Function & Feature

The device is one of key part of system. It provides the interface control of Processor, Memory, AGP and SiS962. In power management, it is in compliance with ACPI2.0 and APM1.2.

In memory system, it supports 266MHz DDR devices and 64Mb, 128Mb, 256Mb and 512Mb technologies for x16 devices and x8 devices. By using 512Mb technology, the largest memory capacity possible is 1.0GB

In AGP interface, it uses the internal VGA Controller.

In SiS962 interface, it supports high throughput SiS MuTIOL connection to SiS962 MuTIOL Media I/O.

- a. Bi-directional 16 bit data bus.
- b. Perform 533MB/s bandwidth in 66MHz x 4 mode
- c. Distributed arbitration strategy with enhanced mode of contiguous DMA data streaming
- d. Packet based, pipelining, and split transaction scheme

5.1.2 – PCI Address

The device is internally located on PCI address 0x80000000.(Bus 0, Device 0, Function 0). Please check [Table 3-1](#) for reference.

5.1.3 – Sub-system & Sub-vendor ID

Subsystem ID : 0x8081

SubVendor ID : 0x1043

5.1.4 – DRAM TYPE Registers

The DRAM Type Register defines the type (NBA*NRA*NCA) and side of each pair of DRAM rows. The offset of these registers are 60h~62h. The following is the mapping of the registers.

DRT0(row 0) : 60h

DRT1(row 1) : 61h

DRT2(row 2) : 62h

The supported DDR type

Bank x Row x Column Bank x Row x Column

1x11x8(8MB)	1x13x8(32MB)
2x12x8(32MB)	2x13x8(64MB)
1x11x9(16MB)	1x13x9(64MB)
2x12x9(64MB)	2x13x9(128MB)
1x11x10(32MB)	1x13x10(128MB)
2x12x10(128MB)	2x13x10(256MB)
2x11x8(16MB)	2x13x12(1GB)
2x12x11(256MB)	2x13x11(512MB)

5.2 - SOUTH BRIDGE (SIS962)

5.2.1 – MuTIOL Media I/O

5.2.1.1 – Function

A high bandwidth and mature SiS MuTIOL technology is incorporated to connect SiS650 and SiS962 MuTIOL Media I/O together. SiS MuTIOL technology is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in SiS962 to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from SiS650, and the Multi-threaded I/O Link Encoder/Decoder in SiS650 to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from SiS962.

5.2.1.2 – PCI Address

This device is internally located on PCI address 0x80001000 (Bus 0, Device 2, Function 0). Please check [Table 3-1](#) for reference.

5.2.1.3 – Features

The SiS962 MuTIOL Media I/O integrates the Audio Controller with AC 97 interface, the Ethernet MAC, Three USB 1.1 Host Controllers, One USB 2.0 Host Controller, the IDE Master/Slave controllers, and the MuTIOL Connect to PCI bridges.

The Integrated Audio controller features a 6-channel of AC 97 v2.2 compliance audio to present 5.1-channel Dolby digital material or to generate stereo audio with simultaneous V.90 HSP modem operation.

The integrated Fast Ethernet MAC features an IEEE 802.3 and IEEE 802.3x compliant MAC supporting full duplex 10 Base-T, 100 Base-T functions in G1/G2 states are supported.

The integrated Universal Serial Bus Host Controllers features Three Independent OHCI USB 1.1, One EHCI USB 2.0 Compliant Host controllers with six USB ports.

The integrated Universal Serial Bus Host Controllers features Dual Independent IDE channels supporting PIO mode 0,1,2,3,4 and Ultra DMA 33/66//100/133. The MuTIOL

Connect to PCI bridge supporting 6 PCI master is compliant to PCI 2.2 specification.

The integrated power management module incorporates the ACPI v1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec.v1.1.

5.2.2 – LPC Interface Bridge

5.2.2.1 – Function & Feature

This device contains many other functional units, such as DMA and Interrupt Controller, Timers, Power Management, System Management, GPIO, RTC and LPC Configuration Registers.

5.2.2.2 – PCI Address

This device is internally located on PCI address 0x80001000 (Bus 0, Device 2, Function 0). Please check [Table 3-1](#) for reference.

5.2.2.3 – Specific I/O Base Address (PMBASE)

One specific I/O Base Addresses are defined in this device – PMBase. PMBase is defined in PCI Configuration Space register 0x74~0x75, also called ACPIBase. The registers offset based on PMBase(ACPIBase) are ACPI1.0b compliance, also handles the GPIO pins functions. Current register settings by BIOS are

PMBase Address : *E400h*

5.2.2.4 – Interrupt

This section contains some interrupts configuration and relative PCI registers.

5.2.2.4.1 – SCI Interrupt

SCI IRQ routing is general set to IRQ20(APIC mode)/IRQ9(Non-APIC mode). The relative register is PCI register 0x68. IRQ Selections are described below.

Bit3:0 : 0000b -> IRQ20
 1001b -> IRQ9
 Others are reserved or not available in this system

SCI : IRQ20(APIC mode)/IRQ9(Non-APIC mode)

5.2.2.4.2 – PIRQ[A,B,C,D,E,F,G,H] Routing Control

PIRQA Routing Control Register 0x41
PIRQB Routing Control Register 0x42
PIRQC Routing Control Register 0x43

SOFTWARE SPECIFICATIONS

PIRQD Routing Control Register 0x44
PIRQE Routing Control Register 0x60
PIRQF Routing Control Register 0x61
PIRQG Routing Control Register 0x62
PIRQH Routing Control Register 0x63

The description of bit fields are described below.

Bit7 : Interrupt Routing Enable
1 -> The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]
0 -> The PIRQ is not routed to the 8259.

Bit6~4 : Reserved

Bit3~0 : 0000 = Reserved, 1000 = Reserved
0001 = Reserved, 1001 = IRQ9
0010 = Reserved, 1010 = IRQ10
0011 = IRQ3, 1011 = IRQ11
0100 = IRQ4, 1100 = IRQ12
0101 = IRQ5, 1101 = Reserved
0110 = IRQ6, 1110 = IRQ14
0111 = IRQ7, 1111 = IRQ15

Current BIOS setting is described below (Legacy Mode),

Table 5-1 IRQ Configuration Table

PIN	IRQ	PIN	IRQ
A	11	E	5
B	10	F	6
C	4	G	9
D	3	H	9

5.2.2.4.3 – IRQ Resource Allocation (Legacy Mode)

D1 uses the following table to allocate IRQ resources.

Table 5-2 IRQ Resources Allocation (Legacy Mode)

IRQ	ALLOCATION	IRQ	Allocation
0	System Timer*	8	CMOS RTC
1	Keyboard	9	SCI
2	Cascade Interrupt Controller	10	PCI Device
3	PCI Device	11	PCI Device
4	PCI Device	12	Mouse
5	PCI Device	13	Numeric Data Processor
6	Floppy Controller	14	Primary IDE Controller*

SOFTWARE SPECIFICATIONS

7	LPT1	15	Secondary IDE Controller*
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* :

INTERNAL ALLOCATION

5.2.2.4.4 – Serial IRQ

Set serial IRQ in continuous mode.

5.2.2.5 – DMA Configuration

The SiS962 supports two types of DMA: LPC, and DDMA. LPC DMA and PC/PCI DMA use the SiS962 DMA Controller.

D1 uses LPC DMA I/F for ECP and Floppy because ITE IT8705F Super I/O is used to support those functions.

Table 5-2 DMA Resource Allocation

Channel	Allocation	Channel	Allocation
0	Reserved	4	Cascade
1	ECP	5	Reserved
2	Floppy	6	Reserved
3	ECP	7	Reserved

5.2.2.6 – Sub-function Devices Enabled/Disabled

The following internal devices are used in D1 design. Registers in SiS962 are used to enable or disable the corresponding device.

Table 5-3 Device can be Enabled/Disabled List

	Description
1	USB1.1 OHCI(D2,F0)
2	USB1.1 OHCI(D3,F1)
3	USB1.1 OHCI(D3,F2)
4	USB2.0.EHCI(D2,F3)
5	AC97 Modem(D2,F6)
6	AC97 Audio(D2,F7)
7	SMBus Controller(D2,F1)
8	LAN Controller(D2,F8)
9	IDE Controller(D2,F5)

5.2.3 – IDE Controller

5.2.3.1 – Function and Feature

SOFTWARE SPECIFICATIONS

The SiS962 IDE controller features two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low.

The SiS962 IDE controller supports both compatibility mode and native mode IDE interface. In native mode, the IDE controller is a fully PCI compliant software interface and does not use any legacy I/O or interrupt resources.

The IDE interface of the SiS962 can support several types of data transfers:

PIO(Programmed I/O) : CPU is in control of the data transfer.

DMA : DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the SiS962. This protocol off loads the CPU from moving data. This allows higher transfer rate of up to 16MB/s.

Ultra DMA/33 : DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33MB/s.

Ultra DMA/66 : DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 66 MB/s.

Ultra DMA/100 : DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s.

5.2.3.2 – PCI Address

This device is internally located on PCI address 0x80001500 (Bus 0, Device 2, Function 5). Please check [Table 3-1](#) for reference.

5.2.3.3 – Sub-System ID and Sub-vendor ID

Subsystem ID : 0x8084

SubVendor ID : 0x1043

5.2.4 – Audio (Realtek ALC650)

5.2.4.1 – Function & Feature

D1 uses the internal AC97 Host Controller of SiS962. It is compliance with AC97 2.2. The SiS962 AC'97 Controller features include :

- a. 6 Channel of AC97 Audio to Present 5.1-channel Dolby Digital Material (Found in DVD Movies) or to Generate Stereo Audio with V9.0 HSP-Modem Operation.
- b. 4 Separate SDTAIN pins supporting multiple Audio Codecs and one Modem Codec.
- c. Effectuating the Realization of 5.1 Channel Dolby Digital Material in Theater Quality Sound.
- d. Support Audio and Modem function with Multithreaded I/O link mastering

5.2.4.2 – PCI Address

This device is internally located on PCI address 0x80001700 (Bus 0, Device 2, Function 7). Please check [Table 3-1](#) for reference.

5.2.4.3 – Specific I/O Base Address

Audio CODEC Register Base Address.
Audio OPR Base Address.

CODEC Register and OPR set to 9400h and 9000h respectively by system BIOS as default value.

5.2.4.4 – Sub-system ID and Sub-vendor ID

Subsystem ID : 0x8095
SubVendor ID : 0x1043

5.2.5 – USB

5.2.5.1 – Function and Feature

The SiS962 contains three USB 1.1 Host controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of six USB ports. Over-current detection on all six USB ports is supported, and an USB 2.0 EHC Host controller. On D1, it uses two USB Host Controllers and supports 4 USB ports.

5.2.5.2 – PCI Address

These four controllers are internally located on PCI address 0x80001800, 0x80001900, 0x80001a00 and 0x80001b00 (Bus 0, Device 3, Function 0/1/2/3). Function 3 is EHCI and others are OHCI Please check [Table 3-1](#) for reference.

5.2.5.3 – Sub-System ID and Sub-Vendor ID

Subsystem ID : 0x8084
SubVendor ID : 0x1043

5.2.6 – Modem (Lucent)

On D1, it also uses AC97 2.2 protocol to communicate with Modem codec. Please refer section [5.2.4](#).

5.2.6.1 – PCI Address

This device is internally located on PCI address 0x80001600 (Bus 0, Device 2, Function 6). Please check [Table 3-1](#) for reference.

5.2.6.2 – Specific I/O Base Address

Modem CODEC Register Base Address.

Modem Operating Register Address.

CODEC and Operating Register base address are set to a000h and 9800h respectively by system BIOS as default value.

5.2.6.4 – Sub-system ID and sub vendor ID

Subsystem ID : 0x1616

SubVendor ID : 0x1043

5.2.7 – SMBus Controller

The SiS962 provides a System Management Bus (SMBus) Specification, Version 2.0-compliant Host Controller as well as an SMBus Slave Interface. The Host Controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The SiS650 is also capable of operating in a mode in which it can communicate with I²C* compatible devices.

5.2.7.1 – PCI Address

The SMBus Host Controller is internally located on PCI Address 0x80001100 (Bus 0, Device 1, Function 1). Please check [Table 3-1](#) for reference.

5.2.7.2 – SMBus Slave Devices

The device which can be accessed through SMBus is called slave device.

In this platform, there are three devices commonly using the same smb. bus.

They are listed below.

DDR SDRAM SPD on Row0

Clock Generator ICS 952003AF

5.2.7.3 – Specific I/O Base Address

0xe600

5.3 – VIDEO (SiS650M)**5.3.1 – Function and Feature**

SiS650M bundled VGA are designed in the D1 platform. It has no integrated memory and supports memory shared with system DDR in the range 4MB to 128MB. The general features of SiS650M VGA are depicted below.

1. High performance 3D accelerator with 2 Pixel/4 Texture, and a 128 bit 2D accelerator with 1T pipeline BITBLT.

SOFTWARE SPECIFICATIONS

2. Video Accelerator and advanced hardware acceleration logic to deliver high quality DVD playback.
3. NTSC/PAL video encoder with Macro Vision Ver.7.1.L1 option for TV display.
4. The Primary CRT display and the extended secondary display (TFT LCD) features the Dual View Capability in the sense that both can generate the display in independent resolutions, color depths, and frame rates.
5. Two separate buses, Host-t-GUI in the width of 64 bit, and GUI-t-Memory Controller in the width of 128 bit are devised to ensure concurrency of Host-t-GUI streaming, and GUI-t-MC streaming.

5.3.2 – PCI Address

This device is internally located on PCI address 0x80010000 (Bus 1, Device 0, Function 0). Please check [Table 3-1](#) for reference.

5.3.3 – LCD Panel ID

Only one type of LCD panel are used in the platform.

5.3.4 – VGA Callback Function

VGA BIOS defines one callback function. Please see following Table.

Table 5-5 VGA Callback function (AX=F401)

BL	Function
05h	Return: MB memory clock, MB bus clock freq, Panel ID, Display Device Select, TV Display Device Select, TV NTSC/PAS Display Select, LCD Expanding/Non-Expanding...etc. Refer to SiS650M UVMA function Spec for more detailed

5.3.5 – Sub-system ID and Sub-vendor ID

Subsystem ID : 0x1612

SubVendor ID : 0x1043

5.4 – LAN (BROADCOM BCM4401KFB)

5.4.1 – Function and Features

Integrated Fast Ethernet MAC Controller

1. Multithread I/O link Mastering with Read/Write Concurrent transaction
2. IEEE 802.3 and 802.3x Standard compatible
3. Supports full duplex 10base-T, 100base-Tx, 1Mb/s & 10Mb/s Home Networking
4. Support ACPI v1.0b and PCI Power Management v1.1 Standard

SOFTWARE SPECIFICATIONS

5. Support 5 Wake-up Frame, Magic Packet wake-up function at G1/G2 state
6. EEPROM free MAC address store scheme

5.4.2 – PCI Address

This device is internally located on PCI address 0x80007800 (Bus 0, Device 15, Function 0). Please check *Table 3-1* for reference.

5.4.3 – PXE2.0 (bootrom support)

BIOS supports boot from LAN that meets PC2001 requirement.
Bootrom is combined into system ROM image to support boot from LAN.

5.4.4 – Sub-system ID and Sub-vendor ID

Subsystem ID : 0x80a8
SubVendor ID : 0x1043

5.5 – CARDBUS (ENE CB710)

5.5.1 – Function and Features

The ENE CB710 is the single chip solution offering one PCI bus-PC card bridge.

5.5.2 – PCI Address

The CARDBUS is internally located on PCI address 0x80005000, 0x80005100 (Bus 0, Device 16, Function 0/1).

5.5.3 – Specific I/O Base Address & Memory I/O Base Address

5.5.4 – Sub-system ID and Sub-vendor ID

Subsystem ID : 0x1724
SubVendor ID : 0x1043

6. Keyboard

7. Setup Menu

D1 system BIOS allows users to change some system hardware/function settings during POST (power on self test) stage, users may hit DEL key to enter SETUP mode in POST, the setup feature is categorized into 5 menus described as below:

Main menu describes system overall information with some user changeable setting, it contains below items:

7.1 – MAIN MENU

System Time: [hh/mm/ss]←current time

System Date: [mm/dd/yy]←current date

IDE drives: Such as hard disk drives and CD-ROM drives. For hard disk and CD-ROM drives BIOS detect them automatically. The users may enter the selected(highlighted) item to get more detailed information, which contains 3 selectable setting:

[Auto]: BIOS default setting.

[User Type HDD]: Users may configure the disk geometry by changing below item:

Translation Methods
Cylinders
Head
Sector
Multi-Sector Transfer
Smart Monitoring
PIO Mode
Ultra DMA Mode

[CD-ROM]:

[None]: Hide the drive.

Installed memory: Total system memory.

7.2 – ADVANCED MENU

In advanced menu the users may configure I/O device resource such as I/O base, interrupt vector or DMA (Direct Memory Access) channel, some auxiliary settings may be changed as well. Detailed I/O device setting are described below:

Default CPU Speed:The CPU clock by manufacture setting, display only.

Max. CPU Speed:The CPU clock while overclock, display only.

Ext. CPU Frequency:The CPU External clock while overclock, or set default for no overclock.

Internal Touchpad: In D1 system a touch pad is installed on the unit, there might be some cases users don't want to use it. The BIOS supports such feature to disable machine's internal pointing device. The default setting is enabled.

I/O Device Configuration:

Parallel Port:[select item]

Set parallel port mode, I/O base address, interrupt vector and DMA channel (if select ECP mode), selectable setting are:

Disabled
378H/IRQ7
278H/IRQ5

The parallel port mode is selectable, available setting are:

Normal
EPP
ECP

SOFTWARE SPECIFICATIONS

The BIOS defaults to ECP mode.

When set to ECP, the DMA channel must be set as below:

ECP DMA Select:[1/3]

The BIOS defaults to channel 3.

7.3 – POWER MENU

This menu contains 4 items.

ACPI Suspend To Ram

CPU Auto Power Saving

Power Up Control

Hardware Monitor

7.4 – BOOT MENU

In this menu users can decide the boot sequence, as long as the device with highest boot priority exists, system BIOS will boot from it, device boot priority is adjusted by pressing “+”, “-” or space key on the selected (highlighted) item. 4 bootable devices for D1 system are listed in this menu (BIOS default boot sequence):

- Removable Device: ← Legacy floppy.
- IDE Hard Drive: ← Hard disk.
- ATAPI CD-ROM: ← CD-ROM
- Removable Device: ← USB floppy / USB ZIP / Flash
- Other Boot Device: ← Network for WfM (Wire for Management)

Onboard LAN Boot ROM:

Enable the function of Network for WfM, default Disabled

7.5 – EXIT MENU

Exit BIOS setup, users may make final decision if they want to save the change just made, or load BIOS default setting, lists are:

- Exit saving changes
- Exit Discarding changes
- Load Setup Defaults
- Discard Changes
- Save Changes

8. Power Management

8.1 – APM 1.2

8.2 – ACPI 2.0

8.3 – SYSTEM SLEEP/SUSPEND AND WAKEUP EVENT

9. PCI Devices SSID/SVIDs

10. Embeded Controller (EC)

10.1 – HOTKEY

Fn key	Description	Available
Fn+F1	Sleep	ACPI
Fn+F5	Brightness Down	ALL
Fn+F6	Brightness Up	ALL
Fn+F7	Panel On/Off	ALL
Fn+F8	LCD+CRT/LCD/CRT Display Switch	ALL
Fn+F10	Volume On/Off	ACPI+ATK0100
Fn+F11	Volume Down	ACPI+ATK0100
Fn+F12	Volume Up	ACPI+ATK0100

10.2 – INSTANT KEY

Key	Description	Available
Email	Invoke Email application	Runtime *1
Internet	Invoke Internet application	Runtime *1
S1	Invoke User defined application/action	Runtime *1
S2	Invoke User defined application/action	Runtime *1

Note:

1. The applications/actions would be invoked only while ATK0100 driver was installed in O/S

10.3 – BATTERY INTERFACE

10.4 – SOFTWARE AUDIO DJ

When user press Audio DJ power button function in power off state, the system runs at a very low power consumption state and play Audio CD automatically in the CDROM/CDRW/DVDROM device. User could also insert Audio CD after Audio DJ power button was pressed. At this time, the whole system can be treated as a CD walkman. User can press the keys described below to control the audio functions or press power button to invoke POST to boot the system.

The Audio DJ keys are also available in O/S when ATK0100 driver installed except Volume Up/Down ,Mute and Audio DJ power button functions

Audio DJ Key	Description	Alternate
Audio DJ Power button	On/Off Audio DJ, not available after system powered up by power button	N/A

SOFTWARE SPECIFICATIONS

Pre track /Volume down	Click to perform Pre track, press for a while to set volume down	Pre track:Left Arrow key Volume Down:Down Arrow key Or F11
Stop/Eject	Stop while playing/Eject while stop	ESC key
Play/Pause	Play/Pause the CD	Space key
Next track /Volume Up	Click to perform Next track, press for a while to set volume up	Next track:Right Arrow key Volume Up:Up Arrow key Or F12
Pre track+Next track	Mute On/Off	N/A

11. SMBIOS 2.3/2.2/2.1

12. PC2001 Compliance

13. Other Features

13.1 – ATK UTILITY

13.1 – BIOS FLASH UTILITY & BIOS CRISIS RECOVERY

Aflash supports BIOS flashing in pure dos mode
Winflash supports BIOS flashing in O/S

13.2 –CPU OVER CLOCK

In “Advanced” group of Setup Screen, the Ext. CPU Frequency is the clock selection for overclock, there're four clocks can be selected for user, 100Mhz is the default and means no overclock, 105/110/115Mhz are for overclock. Once system boot failed, the Ext. clock will be set 100Mhz for next safety Boot. User should down grade the clock setting if the system seems to be unstable due to overclock too much.

The DRAM/AGP/PCI Clocks are always fixed no matter CPU overclock setting changed.

13.3 –THERMAL POLICY

In ACPI mode, the Fans for CPU and system cooling as described below

On / Off(degree)	CPU Fan	System Fan
45 / 35	2000 rpm 20% PWM	2500 rpm 22% PWM
60 / 55	2800 rpm 39% PWM	3400 rpm 41% PWM
70 / 65	3500 rpm 60% PWM	3400 rpm 41% PWM

SOFTWARE SPECIFICATIONS

83 / 75	4500 rpm	5300 rpm
	100%	100%

Thermal shutdown 92 degree